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# AN ANALYSIS OF COMPLEX DOWN MIXING, FILTERING AND DECIMATION IN ACES (U)

by

Eric April

# DEFENCE RESEARCH ESTABLISHMENT OTTAWA
## TECHNICAL NOTE 91-2

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# AN ANALYSIS OF COMPLEX DOWN MIXING, FILTERING AND DECIMATION IN ACES (U)

by

**Eric April**
*Communications Electronic Warfare Section*
*Electronic Warfare Division*

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# ABSTRACT/RÉSUMÉ

## ABSTRACT

This report deals with the problems related to the use of an all-digital HF/VHF wideband receiver in a digital communication intercept system. The high output rates and large bandwidths associated with these receivers result in the need for a post-processing system which can reduce the sampling rate and isolate, in frequency, the bandwidth of interest. Therefore, a means of digitally filtering and mixing the signal to baseband is required. Additionally, a decimation process should be included in the system. General and detailed descriptions of the Mixing, Filtering and Decimation System (MFDS) are given. Simulations of the MFDS are also provided.


## RÉSUMÉ

Ce rapport traite des problèmes reliés à l'utilisation de récepteurs à large bande complètement numériques fonctionnant dans les bandes HF et THF à l'intérieur d'un système d'interception de communications numériques. Les taux d'échantillonnage de sortie excessifs ainsi que les largeurs de bande trop étendues associés à de tels récepteurs conduisent de façon imminente au besoin de conceptualiser un système rattaché à la sortie du récepteur qui réduira le taux d'échantillonnage et isolera, en fréquence, la bande spectrale d'intérêt. Donc, des méthodes numériques de filtrage et de mixage du signal à la bande de base sont requises. De plus, une opération de décimation devra être incorporée au système. Une description générale puis détaillée du Système de Mixage, de Filtrage et de Décimation (SMFD) sont données. La validité du système (SMFD) est évaluée suite aux simulations par ordinateur.

# EXECUTIVE SUMMARY

This report elaborates a system which reduces the sampling rate of a signal coming from a digital wideband receiver (which has ~ 4 MHz bandwidth) and isolates, in frequency, the bandwidth of interest. This system is called the Mixing, Filtering and Decimation System (MFDS). This work was carried out in support of research into the Advanced Communications Electronic Support Measures System (ACES).

The choice for the kind of digital filters to be used in the MFDS is dependent on three specifications: (1) the transition width defined as the spectral region going from the passband to the stopband, (2) the stopband attenuation and (3) preservation of the phase linearity of the filter. From these specifications, an FIR (Finite Impulse Response) filter using a Kaiser window weighting function with 255 taps was selected. Detailed specifications for this filter are contained in the report.

Some typical values associated with the receiver has to be chosen. These include the receiving bandwidth (4 MHz), sampling rate (8 MHz) and scanning range capability (≈ 3-300 MHz ie., HF/VHF bands). From there, an analysis of the overall system has led to the need (mainly due to filter limitations) for two decimation operations such that a new lower sampling frequency is defined. Following this, a detailed description of the MFDS showed three things: (1) how to build a complex bandpass filter, (2) how to perform a complex down-mixing using complex bandpass filters and finally, (3) under which conditions a decimation operation has to be performed in order to prevent aliasing.

Hardware implementation issues are also considered. One important issue is the need for very powerful processors to meet the real-time computational demand. Since common DSP chips (e.g., TMS320C30) do not manifest such power, INTEL iWarp parallel processor boards are proposed as one of the best solutions. In addition, because the signal of interest is not completely isolated from other signals even after two levels of filtering as noted above, further processing will be required. This latter issue will be discussed in a subsequent report.

Finally, computer simulations have been used to prove the validity of the theory used under the MFDS.

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# 1.0 INTRODUCTION

ACES is the acronym for Advanced Communications Electronic Support Measures System. It is a system intended to integrate as much as Electronic Support Measures (ESM) functions. These include signal interception, signal detection, direction finding, modulation recognition, demodulation, etc... This system will utilize all-digital state-of-the-art technologies such as wideband digital receivers and high-speed digital signal processors. For the sake of the present work, a sampling frequency of 8 MHz and a receiving bandwidth of 4 MHz will be assumed for the receiver. It will also be presumed that this digital receiver will be able to sweep the received bandwidth through the whole HF/VHF band.

Trying to process signals at a sampling frequency $f_s$ of 8 MHz is a really difficult task in a real-time digital communication intercept system. In fact, looking at a 4 MHz bandwidth (BW=$f_s$/2) inside the HF/VHF bands leads to the observation of more than one signal of interest (SOI). Assuming the following types of modulation,

a) HF band (3 - 30 MHz): (with 3 KHz channel spacing)
- Upper Side Band (USB) : 2.7 KHz bandwidth
- Lower Side Band (LSB) : 2.7 KHz bandwidth
- On-Off Keying (OOK)/ Amplitude Shift Keying (ASK) : 30 to 50 Bauds ~ 150 Hz bandwidth
- Frequency-Shift Keying (FSK) : 45/100 Bauds, 250/300 Hz bandwidth
- Quadrature Phase-Shift Keying (QPSK), Binary Phase-Shift Keying (BPSK)
- Double Side Band - Suppressed Carrier (DSB-SC)
- Amplitude Modulation (AM)

b) VHF band (30 - 300 MHz): (with 25 KHz channel spacing)
- Frequency Modulation (FM) : deviation 5.0 to 5.6 KHz
- Non-Coherent Frequency-Shift Keying (NC-FSK) : 16 Kbps and 19.2 Kbps for Frequency Hopping

there is a potential of [(27M/3K)+(270M/25K)] ≈ 19800 distinct modulated signals. It is therefore permited to assume a maximum bandwidth per signal of at most 30 KHz. Hence, in order to isolate a SOI from the other signals, a means of digitally filtering and mixing the signal to baseband is required. In addition, the signal must be decimated to provide a signal suitable for further processing by conventional DSP devices such as a TMS320C30. This last operation must give a new sampling frequency $f_{s(new)}$ being approximately twice the bandwidth of any expected SOI bandwidth (say 30 KHz). Therefore, $f_{s(new)}$ will be something around 60 KHz, an attainable speed for conventional DSP chips.

# 2.0 DIGITAL FILTER CONSIDERATIONS

## 2.1 CHOICE OF FILTER

Because it is desired to keep the phase information intact, a linear phase filter has to be used. Therefore, the Finite Impulse Response - FIR - (non-recursive) filter is more appropriate than an Infinite Impulse Response - IIR - (recursive) filter. Also, it offers the advantage of being always stable whereas it is not the case for an IIR filter. Furthermore, the quantization noise is not additive (it is always the same for every output). Some FIR filter characteristics will be discussed below.

First, the sharpness of the filter is proportional to the filter length. The more taps the filter has, the more sharper band edge characteristic it will have. Second, the filter window type dictates the kind of behaviour the filter will have inside the passband region as well as in the stopband region. The Kaiser window (KW) is one of the best types of window because it provides a parameter called beta ($\beta$) which allows a compromise between transition band requirement and stop band attenuation. The KW impulse response is expressed as follows:

$$w(n) = \frac{I_0\left[\beta\sqrt{\left(\frac{M-1}{2}\right)^2 - \left(n - \frac{M-1}{2}\right)^2}\right]}{I_0\left[\beta\left(\frac{M-1}{2}\right)\right]} , 0 \leq n \leq M-1 \tag{1}$$

where M is the filter length (or number of taps), n the sampling instant (an integer) and $I_0$ is the modified Bessel function of order zero. Equations that relate $\beta$ to the stopband attenuation A are

$$\begin{aligned}\beta &= 0 \quad , A < 21\, dB \\ &= 0.5842\,(A - 21)^{0.4} + 0.07886\,(A - 21) \quad , 21\, dB \leq A \leq 50\, dB \\ &= 0.1102\,(A - 8.7) \quad , A > 50\, dB.\end{aligned} \tag{2}$$

From Eq.2, it is easy to compute $\beta$ that corresponds to a stopband attenuation of let's say 80 dB. One will find $\beta = 7.64$. Fig.1 pictures the shape of the impulse response of the KW given in Eq.1 for different $\beta$ (4, 6, 7.64) and M = 255.

It was found that a filter of length M = 255 using a KW with $\beta = 5.66$ provides adequate characteristics to the filter: 60 dB stopband attenuation and a nice sharp band edge as seen in Fig.2. Note that if $\beta$ is reduced, the transition width goes down but the stopband attenuation is also diminished.

The KW gives the filter designer the flexibility that other types of windows like
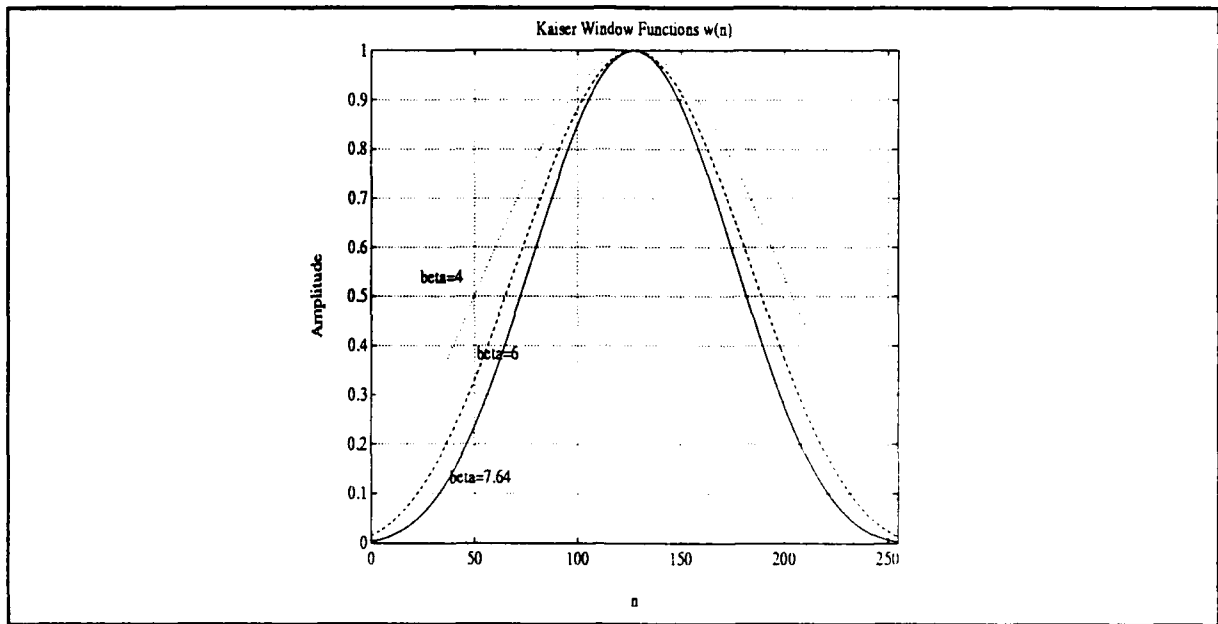
**Figure 1**: Kaiser Window Impulse Response
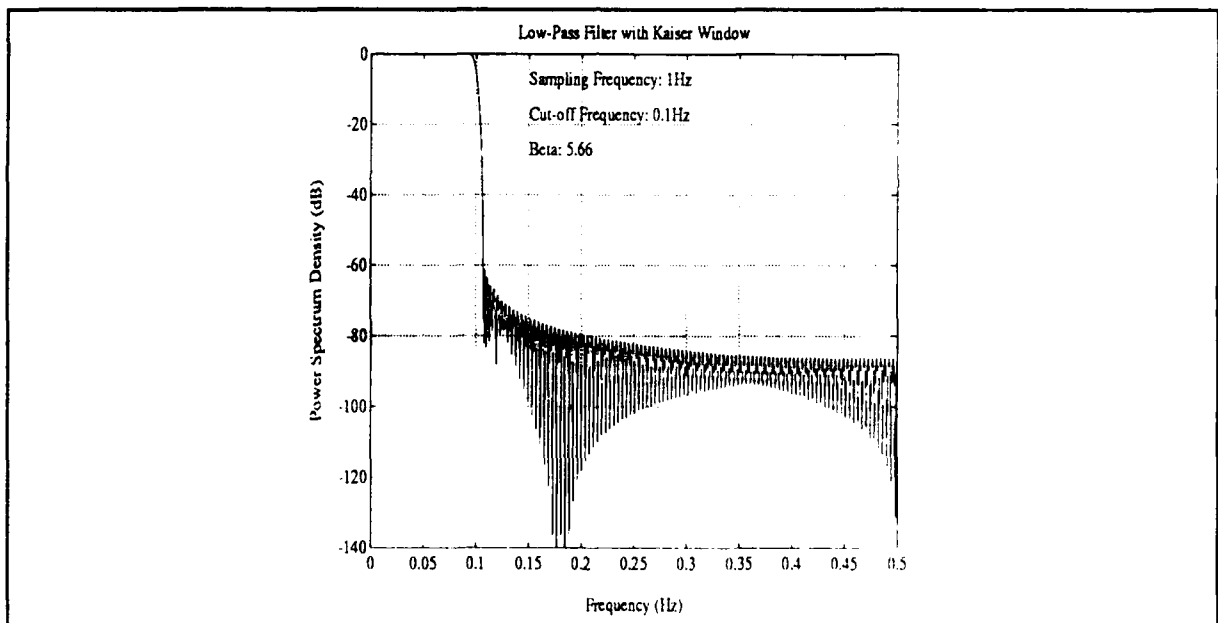


**Figure 2**: Example Of A Low-Pass Filter Using Kaiser Window

Rectangular, Bartlett, Hanning, Hamming and Blackman do not have. All of those have a fixed peak side lobe and a fixed equation available for the transition width of main lobe as shown in Table I.

Recall that the transition width and the peak side lobe for the KW filter design do not only depend on the filter length M but also depends on the parameter β.

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**Table I**: Frequency-Domain Characteristics of Some Window Functions

| Type of Window | Transition Width of Main Lobe | Peak Side Lobe (dB) |
|---|---|---|
| Rectangular | $4\pi/M$ | -13 |
| Bartlett | $8\pi/M$ | -27 |
| Hanning | $8\pi/M$ | -32 |
| Hamming | $8\pi/M$ | -43 |
| Blackman | $12\pi/M$ | -58 |

## 2.2 FILTER LIMITATIONS

Before going further, a more convenient normalized frequency has to be defined. In the digital domain, it is always helpful to use a normalized digital frequency denoted $\theta$ which is equal to $(2\pi \cdot f / f_s)$. From now, it will be easy to go from f to $\theta$ or vice-versa whenever needed (depending on which form is best suited for a particular problem).

The major limitations of the filter are caused by the transition width and the stopband attenuation. The transition width limits how narrow the width of the passband can be. Also, with a KW filter, adjusting $\beta$ such that the stopband attenuation required is met affects the transition width. It is always possible to diminish the transition width by increasing the number of taps M, but in real-time DSP, it is, for a number of reasons, really difficult to do that kind of operation after a certain value of M has been reached. Therefore, M has to be as high as possible but it has a certain practical hardware limitation.

A filter bandwidth limit can be found assuming a KW filter with 255 taps and 60 dB stopband attenuation. For the discussion, the transition width is defined as follows:

$$0 \leq \theta \leq \theta_1 \quad \rightarrow A \leq 0.1 \ dB$$
$$\theta_2 \leq \theta \leq \pi \quad \rightarrow A > 60 \ dB \qquad (3)$$
$$\Delta\theta_{transition} = \theta_2 - \theta_1$$

assuming that a low-pass filter is used. The width of transition is easily found experimentally; for example, a KW low-pass filter having the above characteristics has been designed with a 3 dB cut-off frequency equal to $0.5\pi$ (=$f_s/4$). It gave the following results:

$$\theta_1 = 0.490\pi \ , \ \theta_2 = 0.517\pi \ , \ \Delta\theta_{transition} = 0.027\pi. \tag{4}$$

This last result is of great importance and was found to be independant of the filter cut-off frequency. It means that the filter must add $0.054\pi$ (which is 2 times the transition width) to the bandwidth required for the SOI (something around 30 KHz). This also means that the minimum filter bandwidth is $0.054\pi$.

## 2.3 FILTER SPECIFICATIONS

The specifications for all filters used in next sections are described by the following lines:

| Kaiser Window Filter |
| :---: |
| $\beta = 5.66$ |
| Transition width = $0.027\pi$ |
| Stopband attenuation = 60 dB |
| Filter length: M=255 |

It represents a good compromise between stopband attenuation, transition bandwidth and the filter length M. Note that the transition width as defined in Eq 3 is not a usual way to define it since for filter design purpose, the cut-off frequency is defined as being the 3 dB attenuation point. Therefore, it was found experimentally that for this particular KW filter, going from 0.1 dB to 3 dB attenuation point corresponds to a width of 0.0098π.

From now on, no matter what filter type will be used (low-pass, highpass, bandpass, etc...), the above specifications will always hold.

# 3.0 OVERALL DESIGN STRATEGY

## 3.1 ENERGY DETECTION

A wideband digital receiver located at the front end of an intercept system is assumed to be capable of looking at frequencies from 3 MHz up to at least 300 MHz with 4 MHz of bandwidth at a time. Hence, the first operation after the reception is called Energy Detection (ED). It has to determine if and where a SOI is present inside the 4 MHz bandwidth. If yes, then it detects an approximative center frequency. At the present time, the ED is seen as a system having a frequency resolution of 1 KHz. The Mixing, Filtering and Decimation System (MFDS) receives the approximate center frequency from the ED system and it then begins to isolate the SOI.

## 3.2 MIXING, FILTERING AND DECIMATION SYSTEM

Following the discussion from Section 2, it is known that filtering operations restrict the design of the MFDS. For a sampling frequency of $f_s$ = 8 MHz, the minimum filter bandwidth is $[(0.054\pi \cdot 8M)/2\pi)]$ = 216 KHz. Adding the SOI bandwidth (assumed to be 30 KHz) to this transition bandwidth makes a total filtering bandwidth of 246 KHz. It is therefore obvious that there is no way to go directly from a sampling frequency of 8 MHz to ~60 KHz in only one decimation. It will have to be done in two major similar operations.

Briefly, the steps taken through this process will be the following ones:

1-     ED gives $f_{c1}$ (center frequency) of a SOI.
2-     Complex-mix from $f_{c1}$ to $f_{c2}$ = 500/4 KHz, followed by filtering (bandwidth of complex bandpass filter is BW1 = 246 KHz [1]).
3-     Decimate by 16 to go from $f_{s1}$ = 8 MHz to $f_{s2}$ = 500 KHz, the sampling frequencies.
4-     Complex-mix from $f_{c2}$ to $f_{c3}$ = 83.33/4 KHz and filter (BW2 = 43.5 KHz [2]).
5-     Decimate by 6 to go from $f_{s2}$ = 500 KHz to $f_{s3}$ = 83.33 KHz.

The last sampling frequency, $f_{s3}$ = 83.33 KHz, is the minimum sampling frequency that is feasible to reach in order to insure that a stopband attenuation of 60 dB is respected through all decimation processes and the 30 KHz bandwidth for the SOI has less than 0.1 dB attenuation. Those steps guarantee a very good protection against possible aliasing caused by the mixing and decimation operations. Note that the center frequency is redefined at steps 2- and 4- to be equal to the new sampling frequency divided by 4 (ie., $f_s/4$). The next section will focus on the details of each individual part of this process.

# 4.0 DETAILED SYSTEM DESCRIPTION

## 4.1 COMPLEX FILTER DESIGN

The filter has to be designed first as a low-pass filter with a rectangular window transfer function having the impulse response given by

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[1]   This bandwidth is the total filter bandwidth where the attenuation is less than the stopband attenuation (60dB). Note that the filter bandwidth used for the design is $[30K+(0.0098\pi \cdot 2 \cdot 8M/2\pi)]$ = 108.4 KHz. This result corresponds to the filter bandwidth defined at the 3 dB attenuation points.

[2]   BW2 = $[30K+(0.054\pi \cdot 500K)/2\pi]$ = 43.5 KHz. As in note 1, the 3 dB filter bandwidth is $[30K+(0.0098\pi \cdot 2 \cdot 500K/2\pi)]$ = 34.9 KHz.

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$$h(n) = \frac{\sin\left[\omega_c\left(n - \frac{M-1}{2}\right)\right]}{\pi\left(n - \frac{M-1}{2}\right)} , \quad \begin{array}{l} 0 \le n \le M-1 \\ n \ne \frac{M-1}{2} \end{array} \tag{5}$$

$$h\left(\frac{M-1}{2}\right) = \frac{\omega_c}{\pi} , \text{ if } M \text{ is selected to be odd.} \tag{6}$$

It is already known that the filter length, M, will be odd to insure a symmetric filter spectrum as opposed to an anti-symmetric one when the even length is used. Therefore Eq.6 will always hold. The relationships between $f_c$, $\omega_c$ and $\theta_{BW}$ are shown by the following equations:

$$\omega_c = \frac{2\pi f_c}{f_s} , \quad \theta_{BW} = 2\omega_c \tag{7}$$

where $\theta_{BW}$ is the total filter bandwidth.

Those three last equations define a Rectangular window filter with cut-off frequency $\omega_c$ being in radians and chosen between 0 and $\pi$. Now, the filter impulse response h(n) has to be multiplied by the Kaiser Window impulse response w(n) given in Eq.1. $\beta$ has to be set at 5.66 to provide specifications as discussed earlier. The filter impulse response is then expressed as

$$h_{LP}(n) = h(n)w(n). \tag{8}$$

In the filtering operation, the filter required is a complex bandpass filter. The way of working with such a filter is to separate the real and imaginary part of a complex low-pass filter. The bandpass complex filter is created as follows:

$$h_c(n) = h_{LP}(n)e^{j\theta_c n} = h_r(n) + jh_i(n)$$

$$h_r(n) = h_{LP}(n)\cos(\theta_c n) \rightarrow H_r(\theta) = \frac{1}{2}\left[H_{LP}(\theta - \theta_c) + H_{LP}(\theta + \theta_c)\right] \tag{9}$$

$$h_i(n) = h_{LP}(n)\sin(\theta_c n) \rightarrow H_i(\theta) = \frac{1}{2j}\left[H_{LP}(\theta - \theta_c) - H_{LP}(\theta + \theta_c)\right]$$

where $\rightarrow$ stands for the Fourier Transform operation.

The parameter $\theta_c$ is the bandpass filter center frequency. Note that the power spectrum density (PSD) of $H_r(\theta)$ and $H_i(\theta)$ are identical but their phases are not. See Figs. 3, 4 and 5 for visual representations of respectively $H_r(\theta)$ and $\angle H_r(\theta)$, $H_i(\theta)$ and

$\measuredangle H_i(\theta)$, $H_c(\theta)$ and $\measuredangle H_c(\theta)$.
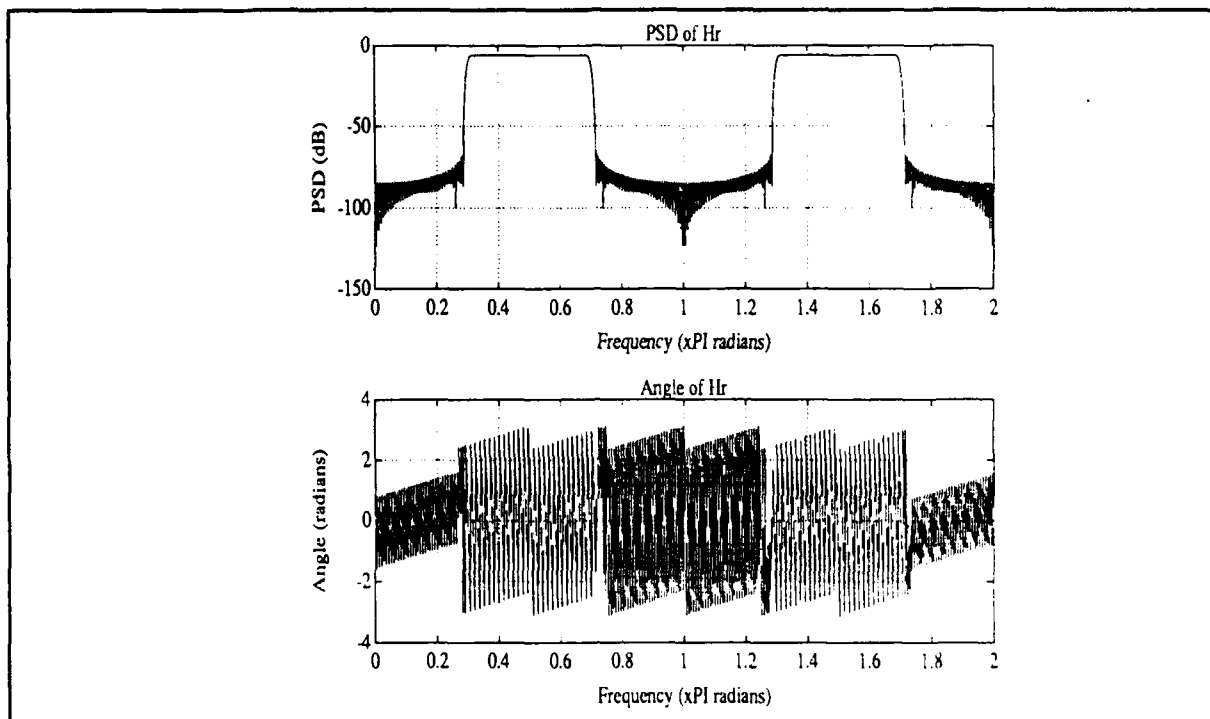


**Figure 3**: Power Spectrum And Phase Plot Of $h_r(n)$

In this example, $\theta_c$ has been chosen to be $0.5\pi$ and the filter bandwidth BW = $0.4\pi$. On the graphs, the value 1 on the x axis coincides with $f_s/2$. The part going from 0 to 1 is the positive frequency side while the part from 2 to 1 is the negative frequency side (2 corresponding to the 0 frequency and 1, the $-f_s/2$ frequency). Recall that in the digital domain, the spectrum is always periodic with a period being equal to $f_s$ (or $2\pi$ in $\theta$ domain).
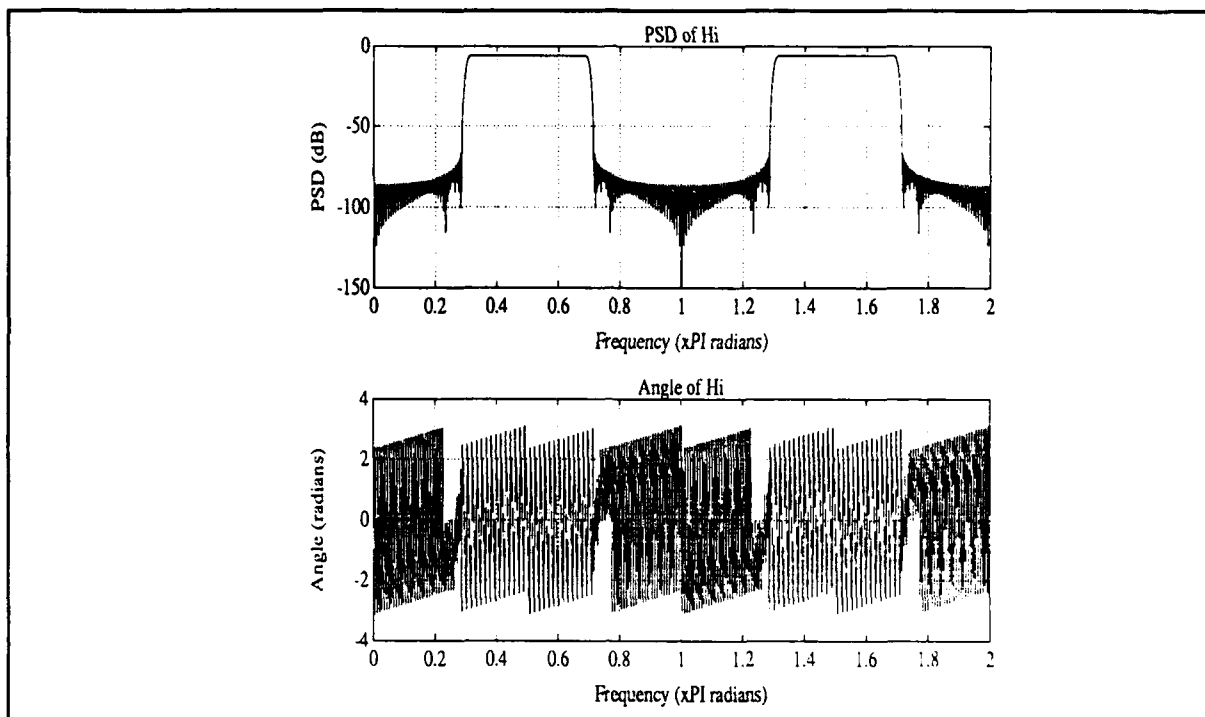
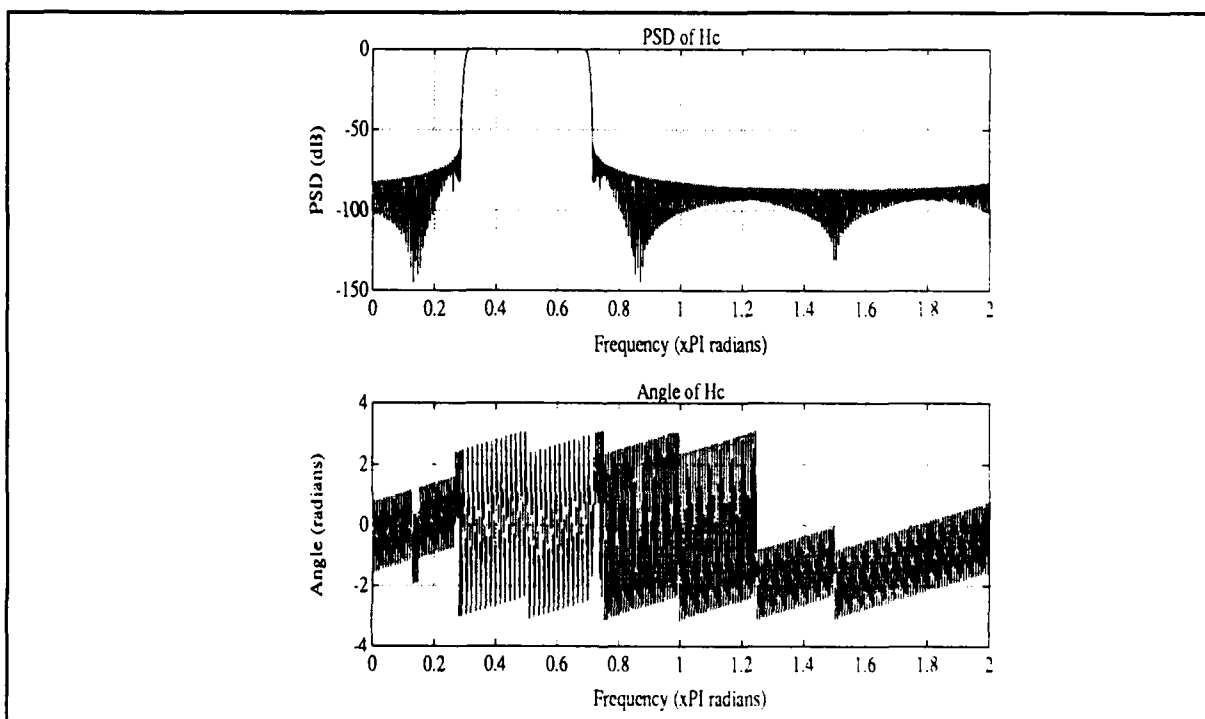**Figure 4**: Power Spectrum And Phase Plot Of $h_i(n)$



**Figure 5**: Power Spectrum And Phase Plot Of $h_c(n)$

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## 4.2 COMPLEX MIXING

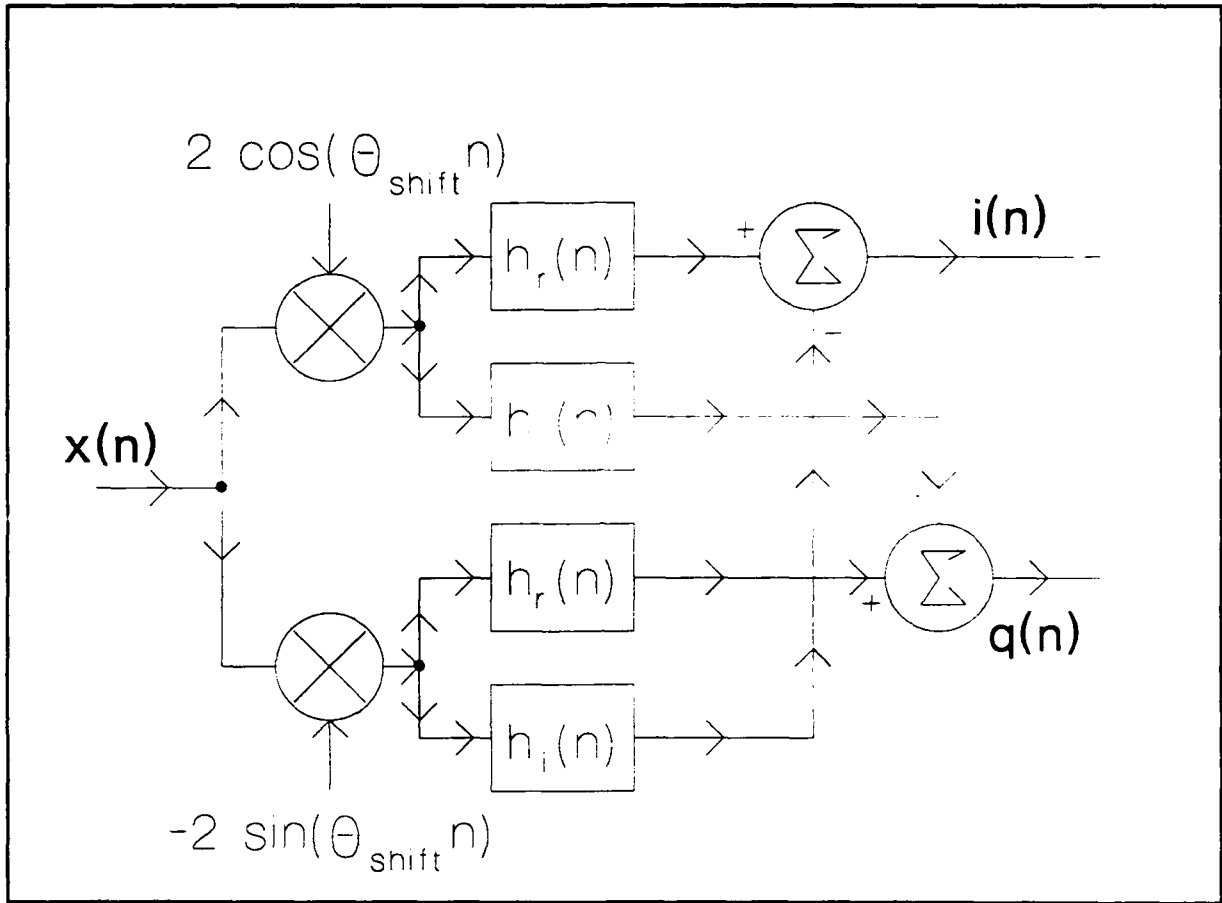The complex spectral shifting block diagram is shown in Fig.6.



**Figure 6**: Complex Mixing Block Diagram

The input, x(n), is the signal to be mixed-down. The output signals are in-phase and quadrature components of the frequency shifted signal, ie., respectively i(n) and q(n). As it can be seen from Fig.6, the input signal x(n) is mixed-down to $\theta_c$ - $\theta_{shift}$ = $\theta_{c(new)}$, a new center frequency, assuming that x(n) has a certain center frequency, $\theta_c$. The filters $h_r(n)$ and $h_i(n)$ are the real and imaginary parts of the complex filter as defined in Eq.9 but with $\theta_c$ now being changed to $\theta_{c(new)}$. Make note that the same filter is used twice within this operation. The bandwidth of the input signal is $\theta_{BW}$. The filter cut-off frequency that has to be used for Eqs. 5 and 6 is based on Eq.7 and is

$$\omega_c = \frac{\theta_{BW}}{2}.$$ 

<div align="right">(10)</div>

The general theory under this complex mixing scheme can be found in Ref.[1], Section 2.2. The next set of equations (Eq.11) briefly presents all the steps one has to go through to arrive at the complex mixing block diagram shown in Fig.6. Notice that the symbol * denotes a convolution operation.

$$h_c(n) = h_{LP}(n) e^{j\theta_{shift} n} = h_r(n) + j h_i(n)$$
$$i'(n) = 2x(n)\cos(\theta_{shift} n)$$
$$q'(n) = -2x(n)\sin(\theta_{shift} n)$$
$$x'(n) = i'(n) + j q'(n) \tag{11}$$
$$y(n) = x'(n) * h_c(n) = \left[ i'(n) + j q'(n) \right] * \left[ h_r(n) + j h_i(n) \right]$$
$$i(n) = \Re\{y(n)\} = \left[ i'(n) * h_r(n) \right] - \left[ q'(n) * h_i(n) \right]$$
$$q(n) = \Im\{y(n)\} = \left[ i'(n) * h_i(n) \right] + \left[ q'(n) * h_r(n) \right]$$

As one may observe, if q(n) is not wanted, the number of parts could be reduced to half. That will make considerable hardware cost savings when implementing the complete MFDS but that will be discussed later.

### 4.3 DECIMATION

A decimation is a fairly simple operation. What seems to be more complex constitutes any process preceding it. The conditions have to be such that no aliasing can arise under the decimation. Therefore, a special care should be taken during the mixing and filtering processes as explained in Section 3. Also, the decimation factors have to be scrupulously chosen. In Section 3.2, those factors were determined to be 16 and 6. Those values are selected to maximize the sampling frequency reduction without affecting the SOI bandwidth.

To decimate the signal by 16 or 6, the samples have to be picked 1 every 16 or 1 every 6 samples of data respectively.

## 5.0 COMPLETE SYSTEM IMPLEMENTATION

### 5.1 BLOCK DIAGRAM

The block diagram of the MFDS is shown in Fig.7. It basically reproduces what has been defined in Section 3.2.

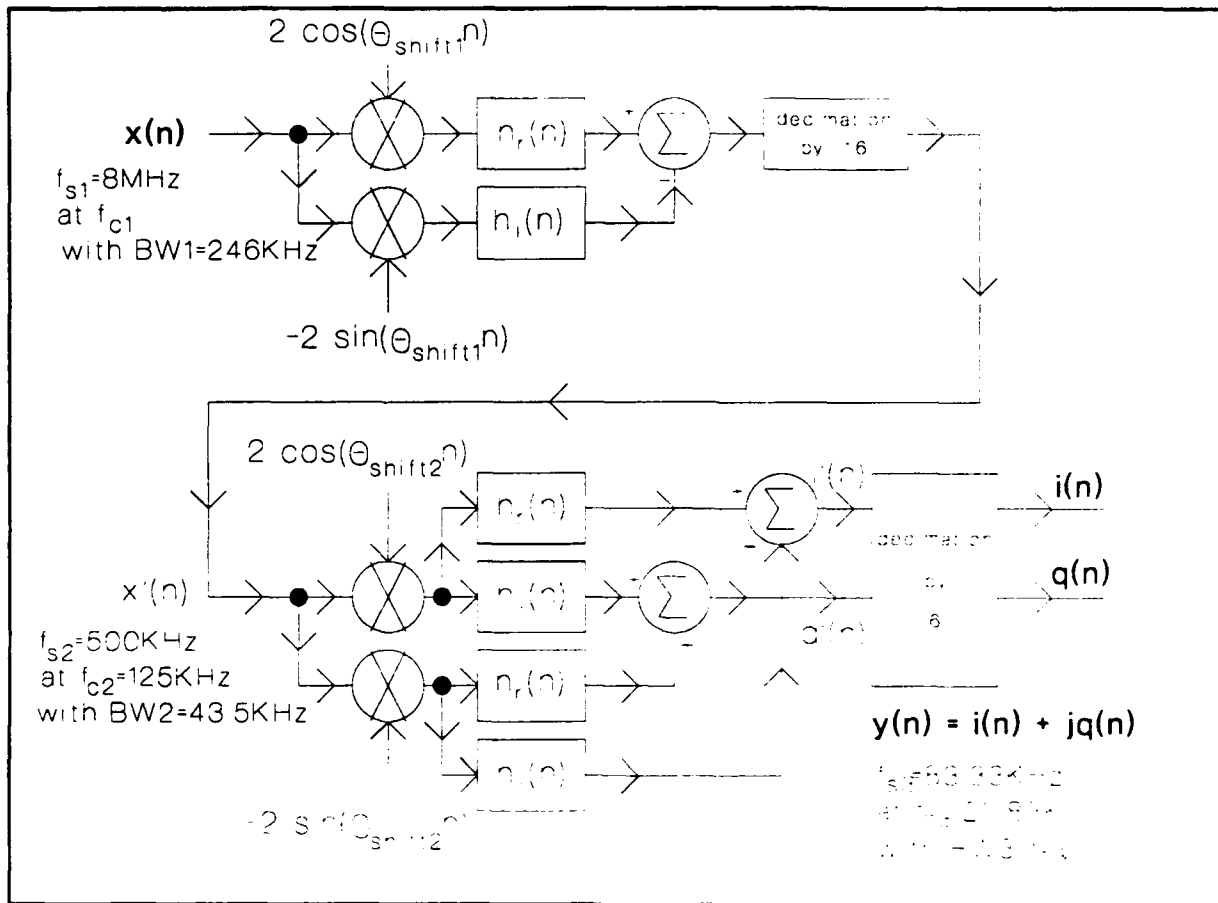To compute the shifting frequencies, $\theta_{shift1}$ and $\theta_{shift2}$, Eq.12 is used, ie.,

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**Figure 7:** Block Diagram Of Complete MDFS

$$\theta_{shift1} = \frac{2\pi\left(f_{c1} - f_{c2}\right)}{f_{s1}}$$

$$\theta_{shift2} = \frac{2\pi\left(f_{c2} - f_{c3}\right)}{f_{s2}} = \frac{2\pi\left(125 - 20.83\right)}{500} = 0.41668\pi$$

(12)

## 5.2 DISCUSSION

The upper part of the block diagram shown in Fig.7 represents the first decimation process changing a sampling frequency of 8 MHz to 500 KHz. This part only needs to produce the in-phase component since the quadrature component is not required as the input to the second decimation process (lower part of Fig.7). As a result, half the filters may be dropped from the first decimation. The second decimation changes the 500 KHz sampling frequency to 83.33 KHz and provide outputs that are the in-phase and quadrature components, i(n) and q(n). Let's look more in detail at the hardware speed requirements for each part.

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The two first mixers need to compute one multiplication in $[1/8M] = 125$ ns. Most common DSP processors can do that job easily. Next, the two filters have to calculate the following:

$$FilterOut_n = \sum_{m=0}^{M-1} b_m FilterIn_{n-m} \tag{13}$$

where $b_m$ are the filter weights. As seen from Fig.7, it looks like the filter outputs data at the same rate as it comes in ie., 8 MHz. But, the filtering and decimating processes can be incorporated such that the filter output rate could be $f_{s2}$, 500 KHz. To do so, the filter computes an output data at { n=0,16,32,... }. Therefore, it must have a queue to keep buffered 16 data before processing them. Hence, the equation will be:

$$FilterOut_n = \sum_{m=0}^{254} b_m FilterIn_{n-m} \; , \; n = 0,16,32,... \tag{14}$$

Eq.14 involves M (=255) multiplications and M additions. Therefore, 2M operations must be performed so that it takes $[1/(500K \cdot 2 \cdot 255)] = 3.92$ ns / operation for each filter. At best, assuming a processor able to do add/multiply in the same instruction, then it would take $[3.92ns \cdot 2] = 7.84$ ns / instruction. Actual common DSP chips are not able to process signals at that speed (eg., TMS320C30 has 60 ns single instruction cycle). Some state-of-the-art processor boards like the Intel iWarp processor boards (not considered here as common DSP boards) could be an alternative but they are very expensive. Nevertheless, they are really fast and very flexible. For real-time intensive computation as for DSP applications, those boards are really well designed. Each iWarp processor is composed of a computation agent and a communication agent. These agents are working simultaneously such that transfer delays between two processors are minimized. Thus, making a very powerful parallel computer with iWarp's is something possible. Using TMS family of processors will never reach the degree of parallelism one can attain using iWarp's.

The 500 KHz $h_i(n)$ output data is substracted from the output of the $h_r(n)$ filter. It requires a maximum instruction cycle of $[1/500K] = 2$ µs. Such a speed is easy to reach with a TMS320C30. The same comment applies for the two mixers in the second decimation system. The filtering can be done along with the decimation as in the first decimation system. It is possible to compute the required processing speed ie., $[1/83.33K \cdot 255] = 47$ ns / instruction. Again, use of iWarp processors may be best suited in this case. The two adders/subtractors at the end must work at $[1/83.33K] = 12$ µs / addition.

At the output of the system, i(n) and q(n) are provided at a rate of 83.33 KHz allowing a signal bandwidth equal to 41.67 KHz. A visualization of the whole MFDS process is shown in Fig.8.

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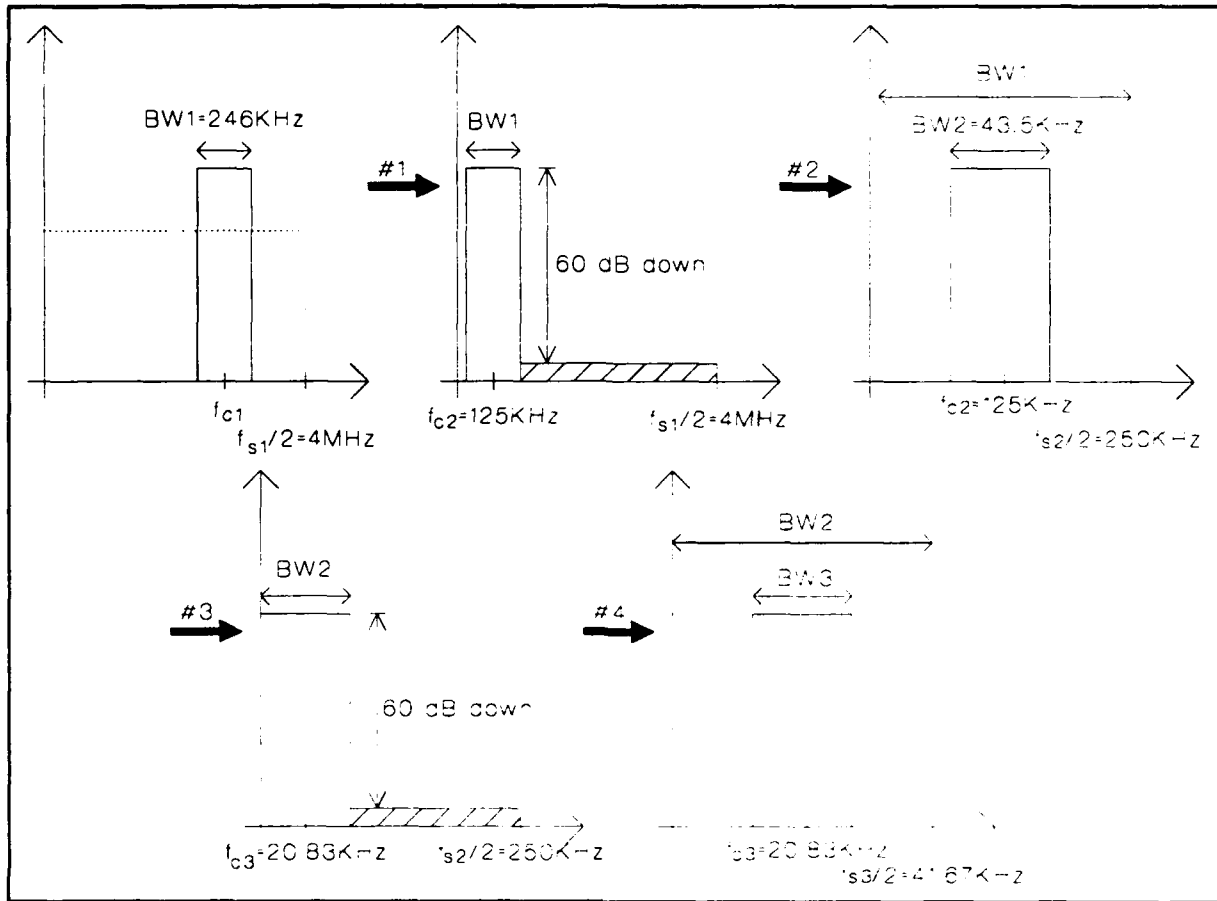
**Figure 8**: MFDS Spectral Visualization

Each numbered arrow symbolizes a particular part of the MFDS operation. Arrow #1 represents the first down mixing and filtering, #2, the first decimation, #3, the second down mixing and filtering and finally, #4 denotes the last decimation. The last graph in the bottom right corner pictures the PSD of i(n) or q(n). The limit of this system resides in a signal band limited to 41.67 KHz. It may therefore be possible to encounter more than one SOI inside this bandwidth according to the possible types of modulation previously described. Additional filterings will have to be made to isolate only one SOI. Nevertheless, the MFDS is fundamentally designed to decrease the data sampling frequency such that a DSP chip like a TMS320C30 will be able to continue any required further processes. Anyhow, the theory behind the MFDS may serve as a reference for complex down mixing and decimation operations. Note from Fig.8 that the signal on the fifth graph is seen as a signal having an unknown bandwidth frequency BW3 and also, $f_{c3}$ constitutes an approximate center frequency. All post-processing is not considered here because it is out of scope of this technical memorandum.

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# 6.0 SIMULATIONS AND RESULTS

## 6.1 SIMULATION SETUP

The present simulation is intended to demonstrate the validity of the theory used under MFDS. For this matter, only one complex mixing, filtering and decimation will be performed instead of two as in MFDS since the operations are the same. Also, the values will not be identical to what was previously discussed. The following describes the simulation conditions:

- The input signal, $x_n$, is a block of data of length 16384 having a sampling frequency of $f_{s1} = 240$ KHz. It is composed of three distinct signals: one is a BPSK signal at a center frequency $f_{c1} = 90$ KHz with a bandwidth of 6 KHz, the second one is an ASK signal at $f_c = 50$ KHz with a bandwidth of 15 KHz and finally the last one is another BPSK signal at $f_c = 110$ KHz with a bandwidth of 10 KHz. The modulation envelopes were generated from digitized samples of an actual voice.

- The first BPSK signal located at $f_{c1} = 90$ KHz and BW1 = 6 KHz will be considered as the SOI to isolate.

- The objective is to take that BPSK signal at a 240 KHz sampling rate, mix it down to a new center frequency $f_{c2} = 7.5$ KHz and decimate it to get a new sampling frequency $f_{s2} = [240K/8] = 30$ KHz (decimation by 8).

- With the same data used to generate the SOI, a BPSK signal with a sampling frequency of 30 KHz, a bandwidth of 6 KHz and a center frequency of 7.5 KHz will be built. Through the simulation, this signal will be called B3 and will serve as a reference to compare to the system output, Yd. Y will stand for the down converted signal before decimation. To compare Y to its expected result, an other BPSK signal called B4 will be generated at $f_{c2} = 7.5$ KHz with a 6 KHz bandwidth and a sampling frequency of 240 KHz.

- For filter design purposes, the 3 dB cut-off frequency is equal to $[6K+(0.0098\pi \cdot 240K/\pi)] = 8.352$ KHz. Also, the total bandwidth for 60 dB attenuation will be $[6K+(0.054\pi \cdot 120K/\pi)] = 12.48$ KHz which has to be lower than $f_s/2$ (15 KHz).

## 6.2 SIMULATION ALGORITHM

The present section describes a complete algorithm illustrating the program steps. It is proposed as a guideline for any software/hardware implementation of a complex mixing, filtering and decimation system.

Step 1:        - Inputs:

$x$ => block of data of length N1=16384
$sf$ => sampling frequency
$cf$ => center frequency of the SOI
$bwf$ => 3 dB bandwidth allowed for filter according to SOI
           bandwidth
$ncf$ => new center frequency
$dr$ => decimation ratio
$M$ => filter length
$\beta$ => beta parameter for KW = 5.66 for 60 dB attenuation

Step 2:        - Complex Mixing:

$\theta_{shift} = 2\pi(cf-ncf)/sf$
$\theta_{ncf} = 2\pi(ncf)/sf$
FOR n=0 to N1-1, DO

$$x_r(n) = 2x[n]\cos(\theta_{shift}n)$$

$$x_i(n) = -2x[n]\sin(\theta_{shift}n)$$

END

Step 3:        - Filter Design:

$\omega_c = \pi(bwf)/sf$
FOR n=0 to [((M-1)/2)-1], DO

$$h[n] = \frac{\sin\left[\omega_c\left(n - \frac{M-1}{2}\right)\right]}{\pi\left(n - \frac{M-1}{2}\right)}$$

$$w[n] = \frac{I_0\left[\beta\sqrt{\left(\frac{M-1}{2}\right)^2 - \left(n - \frac{M-1}{2}\right)^2}\right]}{I_0\left[\beta\left(\frac{M-1}{2}\right)\right]}$$

$$h_{LP}(n) = h(n)w(n)$$
$$h_r(n) = h_{LP}(n)\cos(\theta_{ncf}n)$$
$$h_i(n) = h_{LP}(n)\sin(\theta_{ncf}n)$$

END

$$P = \frac{M-1}{2}$$

$$h_{LP}(P) = \frac{\omega_c}{\pi}$$

$$h_r(P) = h_{LP}(P)\cos\left(\theta_{ncf} n\right)$$

$$h_i(P) = h_{LP}(P)\sin\left(\theta_{ncf} n\right)$$

FOR n=[((M-1)/2)+1] to M-1, DO

$$h_r(n) = h_r(N1-n)$$
$$h_i(n) = h_i(N1-n)$$

END

Step 4:    - Filtering:

$$i = cconv\left(h_r, x_r\right) - cconv\left(h_i, x_i\right)$$
$$q = cconv\left(h_i, x_r\right) + cconv\left(hr, x_i\right)$$

Step 5:    - Decimation:

FOR n=0 to [(N1/dr)-1], DO

$$idec(n) = i(dr \times n)$$
$$qdec(n) = q(dr \times n)$$

END

Step 6:    - Outputs:

i => in-phase output component before decimation
q => quadrature output component before decimation
idec => in-phase output component after decimation
qdec => quadrature output component after decimation

Note that in Step 4, the function "cconv" performs a circular convolution between the two arguments in parenthesis. The output of a circular convolution has the same length of the argument that has the greater length. The formula for a circular convolution is:

$$y(n) = \sum_{m=0}^{M-1} h(m)x\left[MOD(n-m,N)\right].$$

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for n=0,1,...,N-1 where N is the length of x and M, the length of h. The MOD function finds the modulo N value of the first argument. The circular convolution is used here because the operation involves a block of data manipulations instead of a continous real-time data stream.

## 6.3 RESULTS OF SIMULATIONS

In this section, the power spectral density (PSD) of the signals will be compared (in log scale). On the graphs, the following symbols will be used:

Y => PSD of i(n), the in-phase component before decimation.
X => PSD of x(n), the input signal.
Yd => PSD of idec(n), the in-phase component after decimation.
B3 => PSD of directly generated SOI signal at a 30 KHz rate.
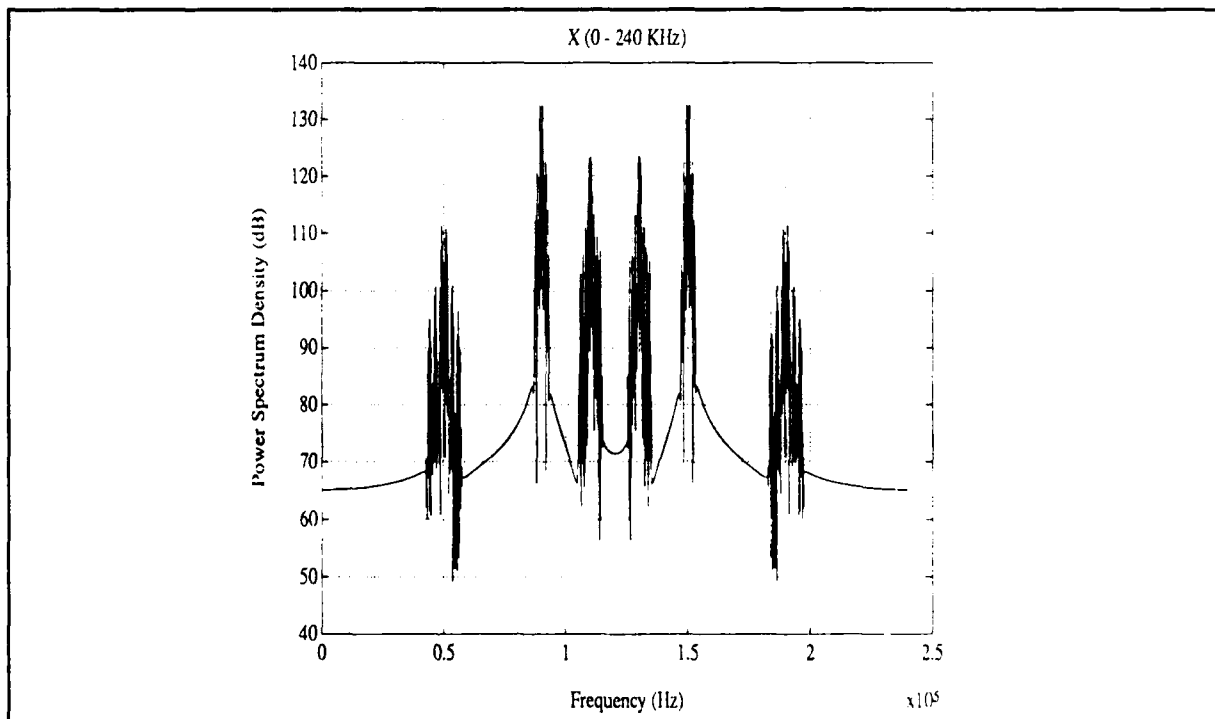B4 => PSD of directly generated SOI signal at a 240 KHz rate.



**Figure 9**: PSD Of Input Signal

As seen from Fig.9, X shows clearly the three distinct signals between 0 and 120 KHz. Also, because the signal is real, the spectral symmetry characteristic can easily be observed. The SOI is in the middle of the three first left signals (ie., at $f_c$ = 90 KHz) and its symmetrical image is seen at $f_c$ = 150 KHz or [150K-240K] = -90 KHz.

The result of the complex mixing and filtering operation, depicted in Fig.10 as Y,

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shows only one non-attenuated signal which is the mixed and filtered SOI at 7.5 KHz. This signal can also be seen at -7.5 KHz or [240K-7.5K] = 232.5 KHz. All the other signals are attenuated by at leat 60 dB. A comparison between Y and B4 is made in Fig.11 but it is hard to make any judgement on the result since only 6 KHz is a bandwidth of interest (BOI). Therefore, a zoom of this particular band (4500 - 10500 Hz) has been illustrated in Fig.12. In those two last figures, Y is seen as a solid line while B4 as a dotted line. From Fig.12, only very tiny discrepancies are noticed. The absolute value of the error between Y and B4 within the BOI is shown in Fig.13. The mean of this error is found to be ~0.4 dB.
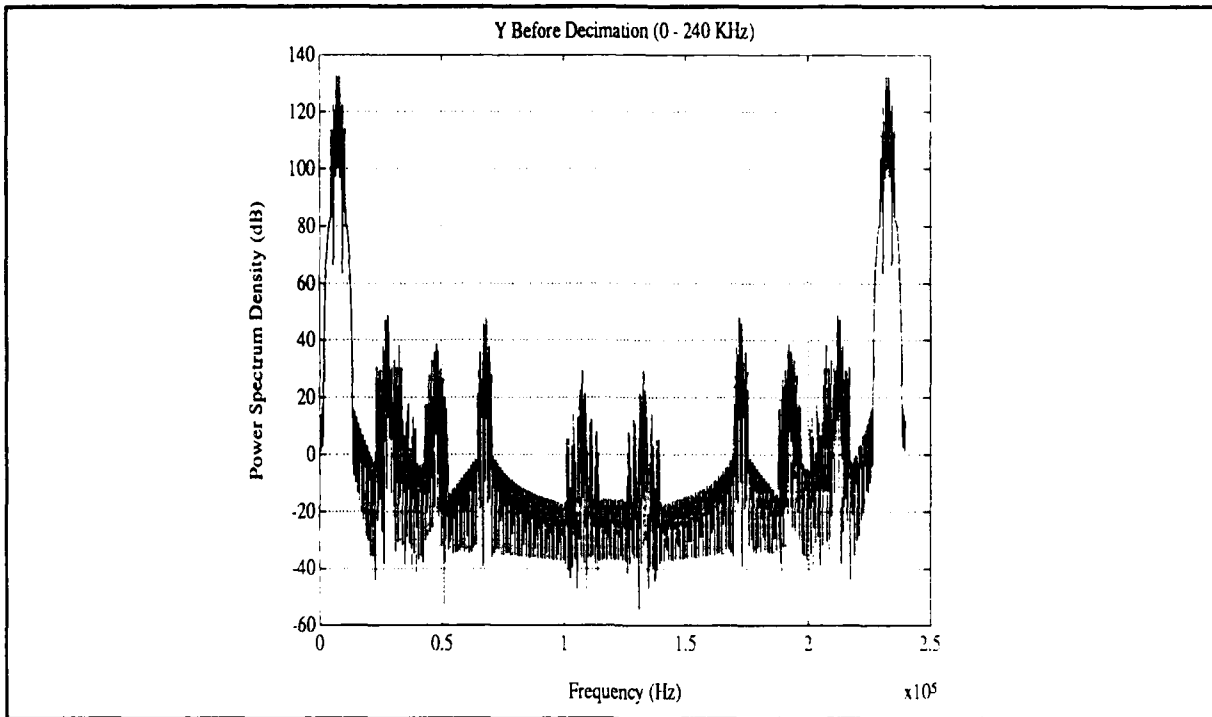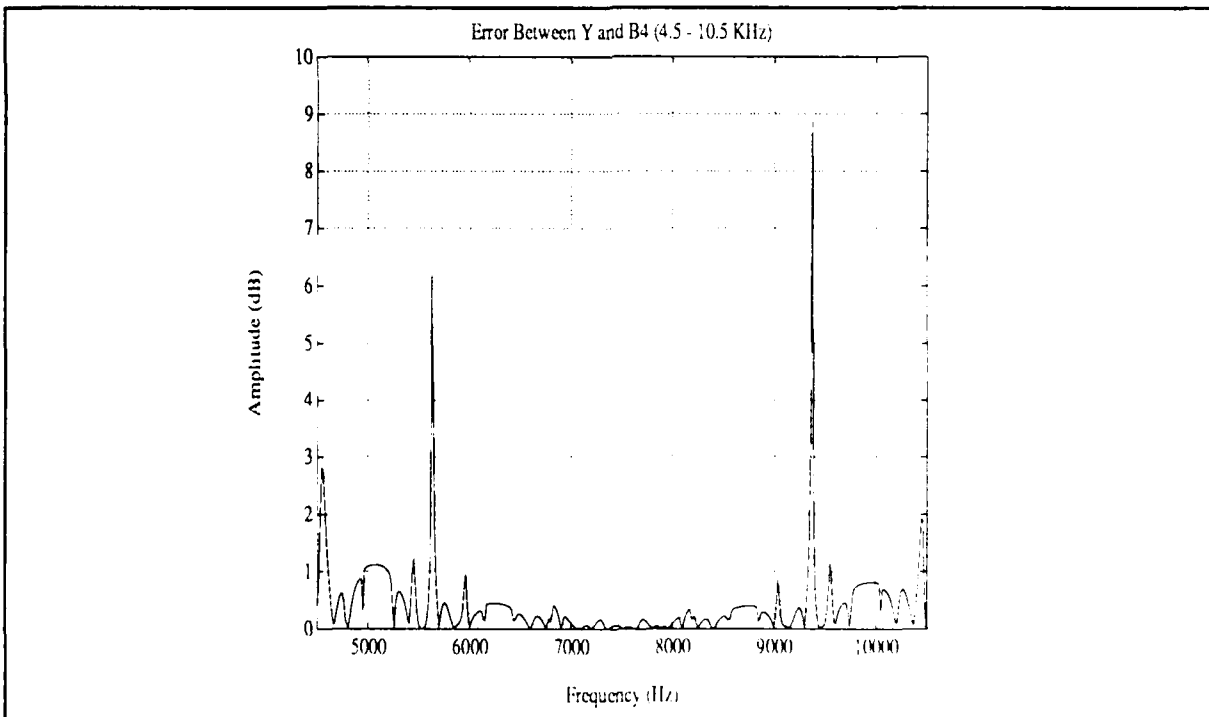
**Figure 10**: PSD Of Real Output Before Decimation
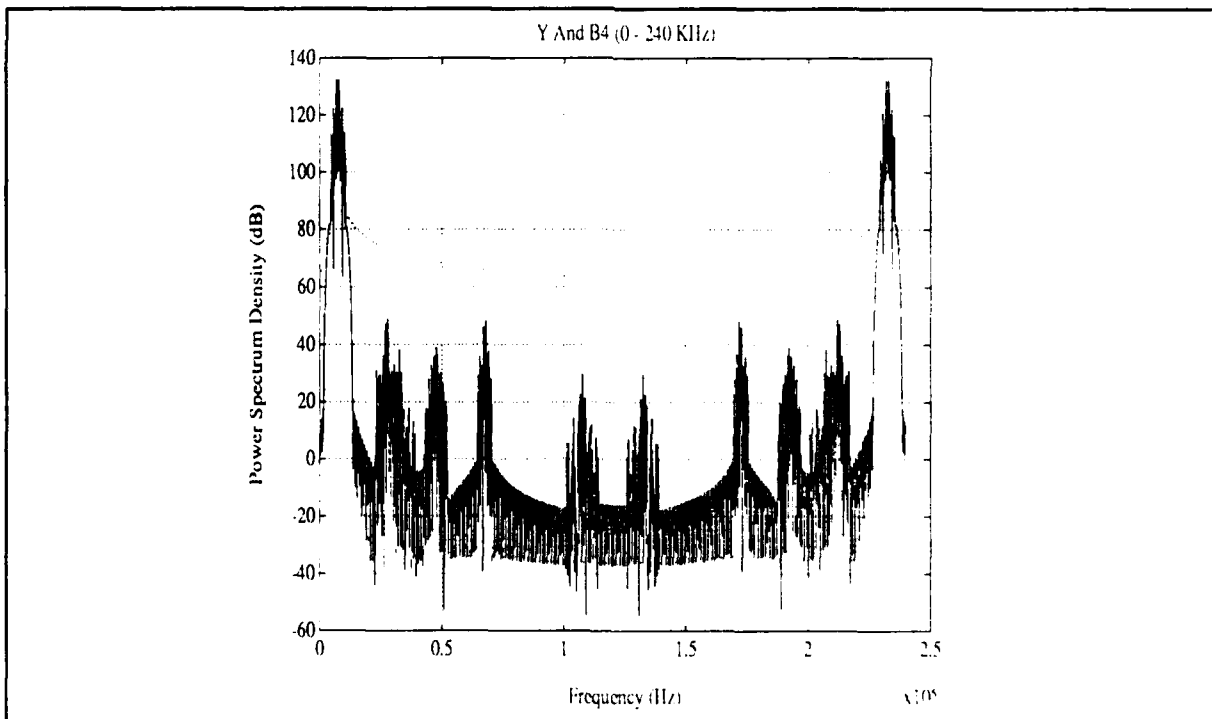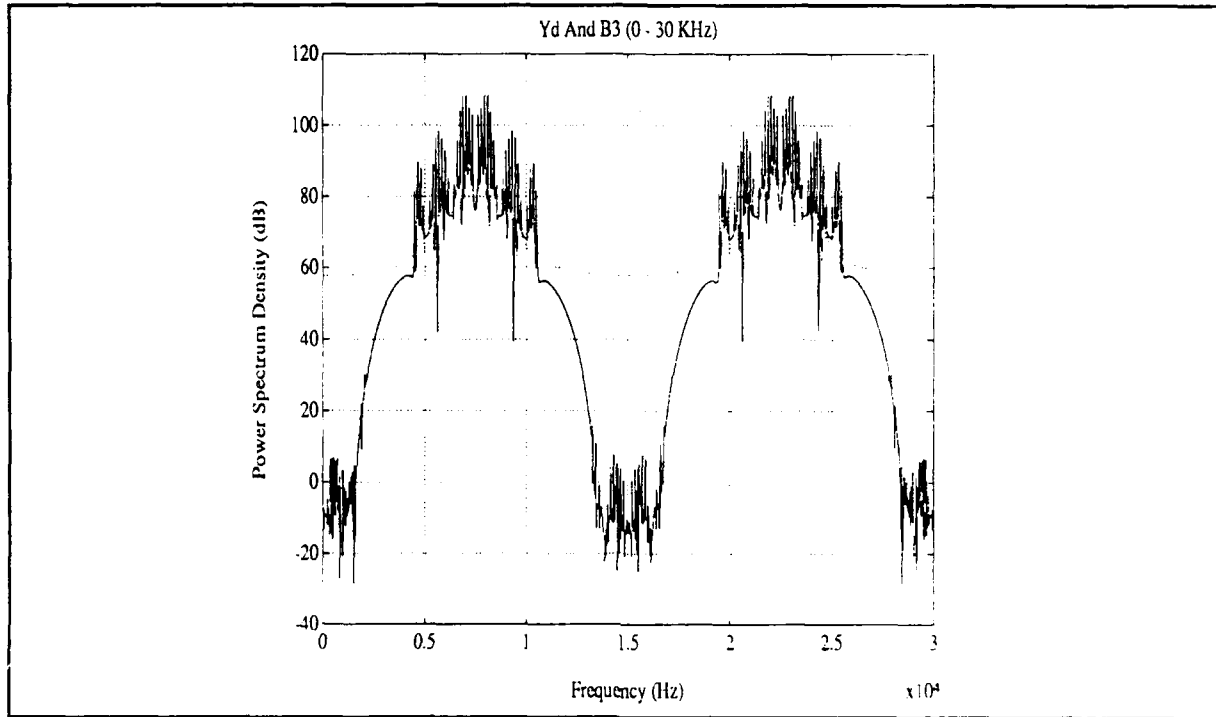


**Figure 11**: Comparison Of Y And B4
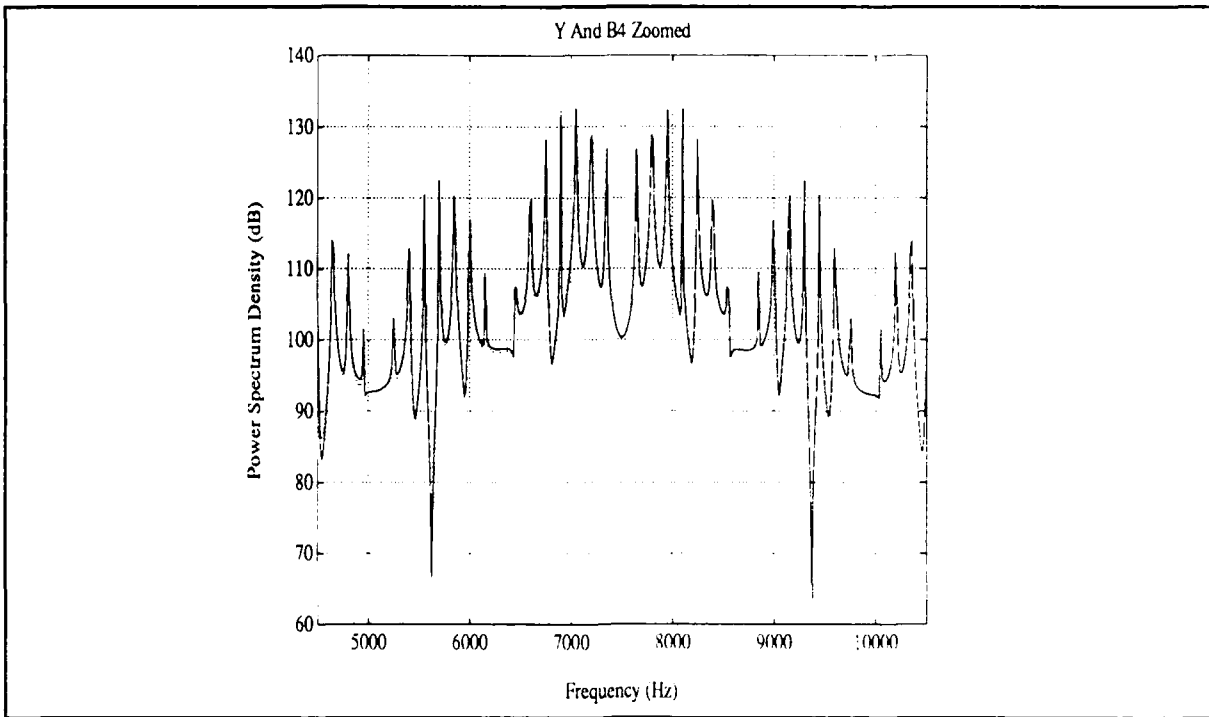
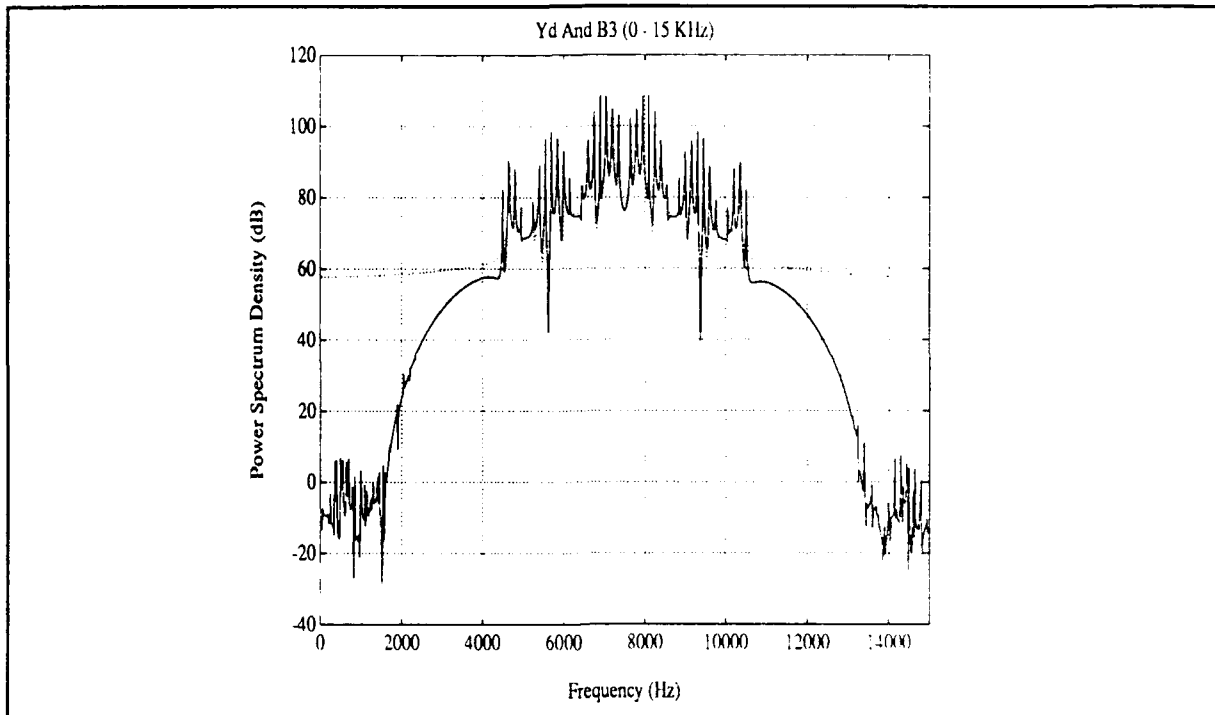**Figure 12**: Comparison Of Y And B4 Within The BOI



**Figure 13**: Error Function Between Y And B4

After the decimation has been performed, Yd and B3 are compared in Fig.14. A closer look at it is taken in Fig.15 (0 - f$_s$/2). Finally, the same frequency band as in Fig.12 is used to compare Yd and B3 in Fig.16. An increased error is observed from there. Now, the mean of the error between Yd and B3 is equal to 1.1487 dB. Again, an error graph within the BOI is drawn in Fig.17.
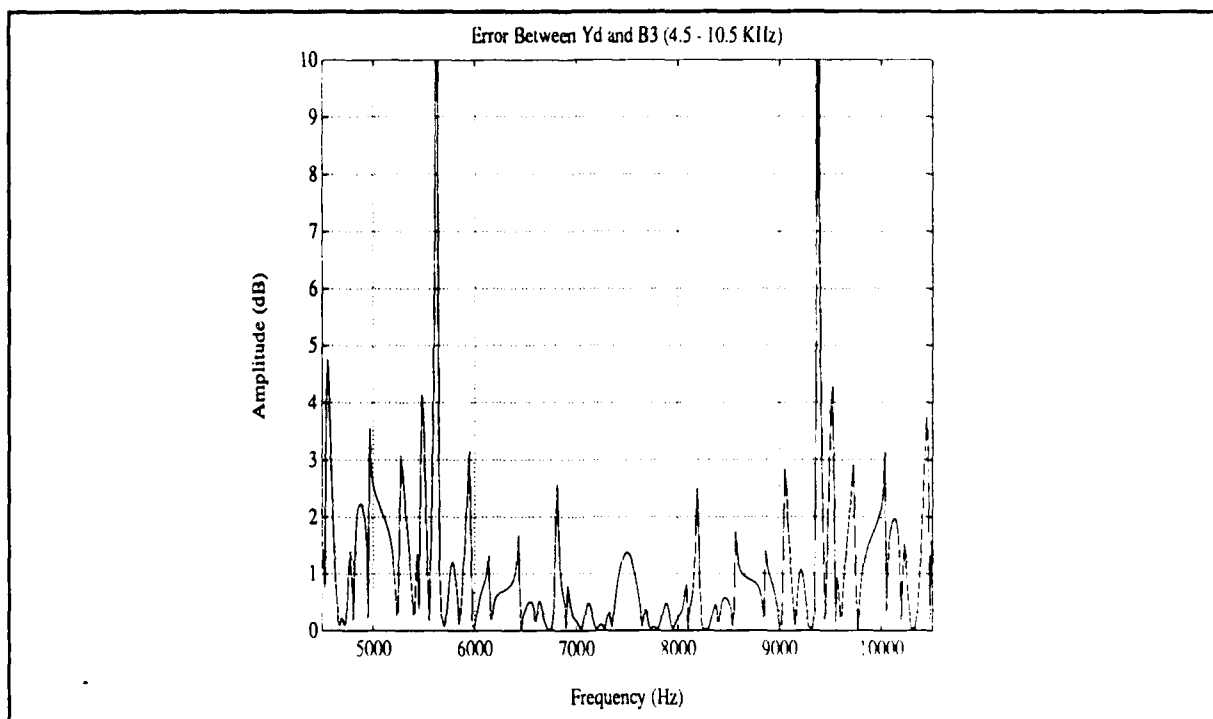


**Figure 14**: Comparison Of Yd And B3

**Figure 15**: Comparison Of Yd And B3 (0 - f$_s$/2)
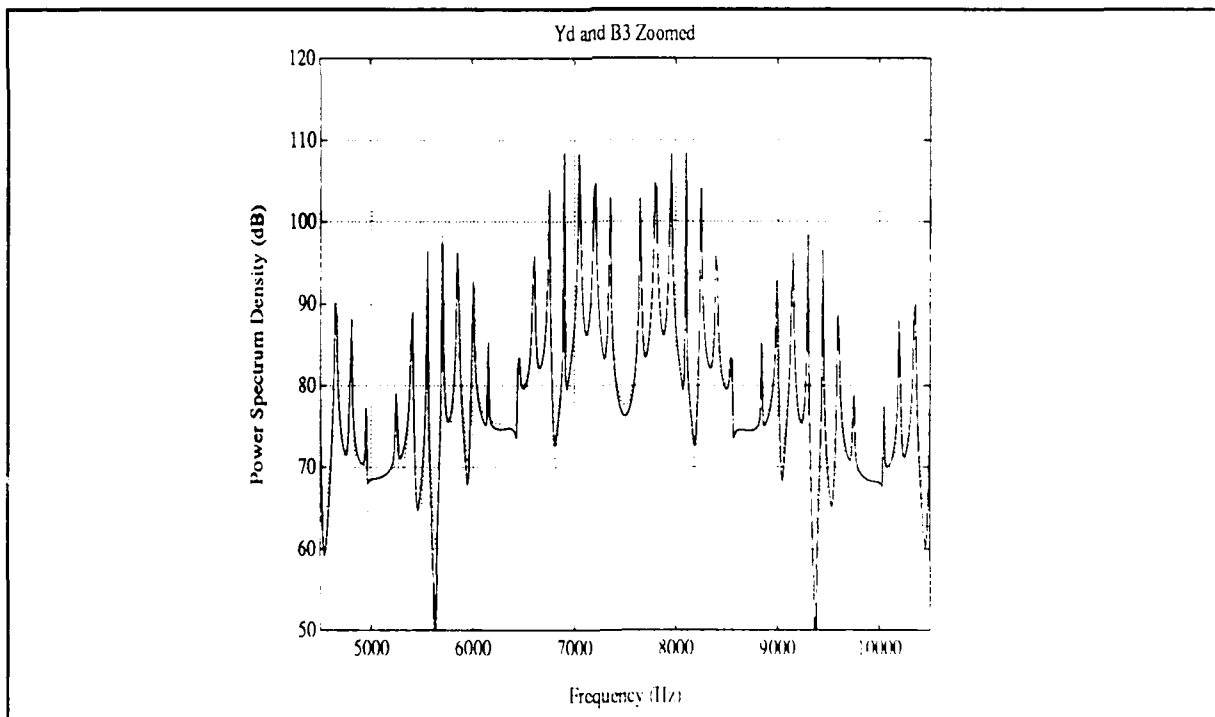


**Figure 16**: Comparison Of Yd And B3 Within The BOI

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**Figure 17**: Error Function Between Yd And B3 Within The BOI

An important observation has to be made from the above results. The value of the error is less meaningful than it appears. As it should be noted from Figs. 12 and 15, the errors appear where the valleys are and not at the peaks. Therefore, errors encountered through the simulation should be considered negligible. Given this fact, the validity of the theory used under MFDS has been confirmed. The observed error is mainly due to the aliasing coming from the 60 dB attenuated signals.

# 7.0 CONCLUSION

This work had two objectives. First, to reduce the sampling frequency given by a digital receiver in the ACES system front end to an attainable speed for a TMS320C30 chip. Second, isolate a SOI without altering it. These two objectives were presented conceptually in Section 6 through computer simulations. Prior to this section, a lot of work was done to determine the filter specifications, define a complex mixing scheme and incorporate a decimation operation to complete an overall system design.

A set of parameters was assumed for the ACES system in order to make the problem as practical as possible at this stage (eg., a receiver with 8 MHz sampling rate). One can also refer to Fig.8. Speed requirements were discussed in Section 5 and from there, it is anticipated that some kind of really fast parallel processing like iWarp boards will be needed. Customized hardware could also be used as an alternative but was not

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mentioned earlier because that approach would be too restrictive.

Briefly, the MFDS can be seen as two non-coherent mixings. Unfortunately, the SOI is not completely filtered at the end and it is therefore envisioned that further processing will be required before studying this particular signal. Consequently, a significant amount of work will be carried on to develop a system called a Digital Coherent Adaptive Down Converter. The output of this system will have to be the SOI only, completely filtered, with a center frequency of 0 and possibly a reduced sampling rate.

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THIS REPORT DEALS WITH THE PROBLEMS RELATED TO THE USE OF AN ALL-DIGITAL HF/VHF WIDEBAND RECEIVER IN A DIGITAL COMMUNICATION INTERCEPT SYSTEM. THE HIGH OUTPUT RATES AND LARGE BANDWIDTHS ASSOCIATED WITH THESE RECEIVERS RESULT IN THE NEED FOR A POSTPROCESSING SYSTEM WHICH CAN REDUCE THE SAMPLING RATE AND ISOLATE, IN FREQUENCY, THE BANDWIDTH OF INTEREST. THEREFORE, A MEANS OF DIGITALLY FILTERING AND MIXING THE SIGNAL TO BASEBAND IS REQUIRED. ADDITIONALLY, A DECIMATION PROCESS SHOULD BE INCLUDED IN THE SYSTEM. GENERAL AND DETAILED DESCRIPTIONS OF THE MIXING, FILTERING AND DECIMATION SYSTEM (MFDS) ARE GIVEN. SIMULATIONS OF THE MFDS ARE ALSO PROVIDED.

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